UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/993,917 | 11/27/2001 | Moshe Stark | 1464-US | 5473 |

24505 7590 07/13/2005

DANIEL J SWIRSKY
PO BOX 2345
BEIT SHEMESH, 99544
ISRAEL

| EXAMINER | |
|---|---|
| DANIELS, ANTHONY J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2615 | |

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/993,917 | STARK, MOSHE | |
| | Examiner | Art Unit | |
| | Anthony J. Daniels | 2615 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No: _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/25/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. The amendment, filed 4/19/2005, has been entered and made of record. Claims 1-44 are pending in the application.

2. Applicant's amendment to the drawings has overcome the examiner's objection.

### *Response to Arguments*

3. Applicant's arguments filed 4/19/2005 have been fully considered but they are not persuasive. In regard to applicant's arguments (see Remarks, p. 3,4), in particular p. 4, where applicant states "...in Figure 3...this [the coupling of SIGNAL line 1 and SIGNAL line 2 onto the output line] results in an outputting a voltage signal that is approximately half the sum of the SIGNAL 1 line voltage and the SIGNAL 2 line voltage...". It is respectfully submitted that examiner has not, in the Non-Final rejection nor in this Final rejection, relied upon the embodiment of Figure 3 in Sauer et al. to reject of any of the claims 1-44. Any embodiments other than Figure 4 that are used as citations are simply used for either structural identification (i.e. pixel elements) or procedural identification (i.e. summing) that is common to each embodiment. In the assumption that the applicant has applied this argument to each embodiment of Sauer et al., the examiner respectfully disagrees with said arguments. Sauer et al. specifically states that the output voltage is the sum of the SIGNAL 1 line voltage and the SIGNAL 2 line voltage (Col. 4, Lines 64-67; Col. 7, Lines 28-32). The assertion of applicant that "...this [the coupling of SIGNAL line 1 and SIGNAL line 2 onto the output line] results in an outputting a

voltage signal that is approximately half the sum of the SIGNAL 1 line voltage and the SIGNAL 2 line voltage..." is clearly incorrect due to the fact that: 1) Sauer et al. **does not**, in any embodiment of his invention, teach averaging the charges output to the output line "30", 2) Sauer et al. teaches that it is desirable to reset SIGNAL line 1 and SIGNAL line 2 before summing onto the output line "30" (Col. 7, Lines 54-57). This implies that the charges are isolated from the capacitors "C11" and "C12"; therefore, the capacitors will not affect the charge on the output line "30", and said output line produces a true sum of the charges on SIGNAL line 1 and SIGNAL line 2. In light of these facts, Sauer et al. is believed to be a proper combination with the references of Kokie et al., Nishida et al., and Pain et al. (see Remarks, arguments from p. 5-10). It is believed that examiner has addressed all arguments from applicant.

***Claim Rejections - 35 USC § 102***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1,12,23,24,26,27,34,35,37,38 stand rejected under 35 U.S.C. 102(b) as being anticipated by Sauer et al. (US # 5,973,311). *Note the interchangeability of lines and columns in claims 24,26,35,37.*

As to claim **1**, Sauer et al. teaches an active pixel image sensor (Figure 2, Figure 4, pixel elements "22" containing transistors "TR11" and "TC11"; *{The active elements, i.e. transistors "TC11", "TR11", define the sensor as an active pixel image sensor.}*) comprising: a plurality of direct injection unit cells (Figure 4, pixel elements "22"; reset "66","68"; *{The reset circuits define the unit cells as charge injection unit cells due to the reset of the charge on the signal*

*lines "1","2".}*), each adapted to generate charge in response to photons incident thereon (Col. 4, Lines 14-21; Col. 7, Lines 27-32); and array elements adapted to sum charge from one or more unit cells at the focal plane of said image sensor (Col. 4, Lines 22-30; Lines 38-44; Col. 7, Lines 27-32).

As to claim **12**, Sauer et al. teaches an active pixel image sensor (Figure 2, Figure 4, pixel elements "22" containing transistors "TR11" and "TC11"; *{The active elements, i.e. transistors "TC11", "TR11", define the sensor as an active pixel image sensor.}*) comprising: a plurality of direct injection unit cells (Figure 1, pixel elements "22"; reset "66","68"; *{The reset circuits define the unit cells as charge injection unit cells due to the reset of the charge on the signal lines "1","2".}*), each adapted to generate charge in response to photons incident thereon (Col. 4, Lines 14-21); and array elements adapted to change resolution of the output image of said image sensor at a focal plane of said image sensor (Col. 4, Lines 14-17; Lines 62-64) by summing the charge generated by one or more unit cells of said plurality of unit cells (Col. 4, Lines 64-67; Col. 7, Lines 14-32).

As to claim **23**, claim 23 is a method claim corresponding to apparatus claim 1. Therefore, method claim 23 is analyzed and rejected as previously discussed with respect to the apparatus claim 1.

As to claim **24**, Sauer et al. teaches a method according to claim 23 and wherein said summing comprises: activating charge transfer transistors of one or more lines of unit cells (Figure 2, "Column Select Line 1" and transistor "TC11"); Col. 5, Lines 23-29; *{Activating column select line 1, in turn, activates the aforementioned transistor of Figure 2.}*); activating one or more columns of unit cells (Figure 4, "Row Select Line 1" and "Row Select Line 2"; Col.

7, Lines 27-32); and combining the charge transferred by activated charge transfer transistors of said activated columns (Col. 7, Lines 24-32).

As to claim **26**, Sauer et al. teaches a method according to claim 23 and wherein said summing comprises activating one line and combining charge of at least two columns thereby to combine charge from at least two unit cells in adjacent columns (Col. 4, Lines 45-67).

As to claim **27**, Sauer et al. teaches a method according to claim 23 and wherein said summing comprises activating U adjacent lines and combining charge of V columns thereby to combine charge from UxV unit cells in a UxV block (Col. 7, Lines 14-32).

As to claim **34**, claim 34 is a method claim corresponding to apparatus claim 12. Therefore, method claim 34 is analyzed and rejected as previously discussed with respect to the apparatus claim 12.

As to claim **35**, the limitations in claim 35 can be found in claim 24. Therefore, claim 35 is analyzed and rejected as previously discussed with respect to claim 24.

As to claim **37**, the limitations in claim 37 can be found in claim 26. Therefore, claim 37 is analyzed and rejected as previously discussed with respect to claim 26.

As to claim **38**, the limitations in claim 38 can be found in claim 27. Therefore, claim 38 is analyzed and rejected as previously discussed with respect to claim 27.

### *Claim Rejections - 35 USC § 103*

5. Claims 2,4,5,13,15,16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Sauer et al. (see Patent Number above) in view of Kokie et al. (US #4,212,034). *Note the interchangeability of rows and columns in claims 2,4,13,15.*

As to claim **2**, Sauer et al. teaches an image sensor according to claim 1 (see above 102(b) rejection) and wherein said array elements comprise: charge transfer transistors (see Figure 2, Reference Number "TC11") adapted to transfer charge when activated (see Col. 5, Lines 23-29); a line decoder (see Figure 4, Reference Number "50"; *{Horizontal Shift Register (50) performs same task as line decoder; see Col. 6, Lines 62-65.}*) adapted to activate charge transfer transistors of one or more lines of unit cells (see Col. 6, Lines 62-65; *{Activating column select line 1, in turn, activates the aforementioned transistor of Figure 2.}*); and a column selector (see Figure 4, Reference Number "48"; *Vertical Shift Register (48) performs same task as column selector; see Col. 6, Lines 60-62.}*) adapted to activate one or more columns of unit cells and to combine the charge transferred by activated charge transfer transistors of said activated columns (see Col. 4, Lines 62-67; Col. 6, Lines 11-20). The claim differs from Sauer et al. in that it requires one charge transfer transistor per unit cell.

In the same field of endeavor, Kokie et al. teaches unit cells (see Figure 1, Reference Numbers "4-1 – 4-4") containing one charge transfer transistor (see Figure 1, Reference Number "5") per unit cell transferring charge from photo detectors (PD4-1 – PD4-4). In light of the teaching of Kokie et al., it would have been obvious to one of ordinary skill in the art at the time the invention was made to include only one charge transfer transistor per unit cell. One transistor per unit cell would decrease space taken up by the unit cell and; subsequently, the array, and one transistor per unit cell would allow for more efficient operation of the array; meaning, not having to activate two transistors to transfer charge from one unit cell as taught by Sauer et al.

As to claim **4**, Sauer et al., as modified by Kokie et al., teaches an image sensor according to claim 2 (see above 103(a) rejection) and wherein said array elements comprise adjacent

column means (see Sauer et al., Figure 2, Clock Input Signals "52" and "54"; Col. 6, Lines 62-65) adapted to indicate to said line decoder to activate one line and to said column selector to combine charge of at least two columns thereby to combine charge from at least two unit cells in adjacent columns (see Sauer et al., Col. 4, Lines 45-67).

As to claim **5**, Sauer et al., as modified by Kokie et al., teaches an image sensor according to claim 2 (see 103(a) rejection above) and wherein said array elements comprise block means adapted (see Sauer et al., Figure 4, Clock Input Signals "52" and "54") to indicate to said line decoder to activate U adjacent lines and to said column selector to combine charge of V columns thereby to combine charge from UxV unit cells in a UxV block (see Col. 7, Lines 14-32).

As to claim **13**, the limitations in claim 13 can be found in claim 2. Therefore, claim 13 is analyzed and rejected as previously discussed with respect to claim 2.

As to claim **15**, the limitations in claim 15 can be found in claim 4. Therefore, claim 15 is analyzed and rejected as previously discussed with respect to claim 4.

As to claim **16**, the limitations in claim 16 can be found in claim 5. Therefore, claim 16 is analyzed and rejected as previously discussed with respect to claim 5.

6. Claims 3,14 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Sauer et al. and Kokie et al. (see Patent Numbers above), and further in view of Pain et al. (US #8,801,258). *Note the interchangeability of rows and columns in claims 3 and 14.*

As to claim **3**, Sauer et al., as modified by Kokie et al., teaches an image sensor according to claim 2, and wherein said array means comprise adjacent line means adapted to provide indications to the line decoder and the column selector (see 103(a) rejection above), but the claim

differs from Sauer et al., as modified by Kokie et al., in that it requires that the provided indications to said line decoder activate at least two adjacent lines and to said column selector select one column thereby to combine charge from the corresponding unit cells in adjacent lines.

In the same field of endeavor, Pain et al. teaches the activation of a column and at least two adjacent lines, noting interchangeability, whereupon the charges are combined from the corresponding unit cells in the at least two adjacent lines (see Col. 2, Lines 59-67, Col. 3, Lines 1-9). In light of the teaching of Pain et al. it would have been obvious to one of ordinary skill in the art at the time the invention was made to activate a column and at least two adjacent lines, whereupon charges are combined from the corresponding unit cells in the at least two adjacent lines. Such activations would allow for two methods of combining charges to be used, 1) activation of two columns and one line and summing as described in claim 4, 2) activation of one column and two lines and summing described by Pain et al.; thus, receiving different signal-to-noise ratios for each method, comparing them, and using the highest to have the sensor operate with an optimal signal-to-noise ratio with little or no change in resolution.

As to claim **14**, the limitations in claim 14 can be found in claim 3. Therefore, claim 14 is analyzed and rejected as previously discussed with respect to claim 3.

7. Claims 6,7,17,18 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Sauer et al., Kokie et al., and Pain et al. (see Patent Numbers above), and further in view of Nishida et al. (US #4,996,600). *Note interchangeability of rows and columns in claims 6,7,17,18. Also note Col. 7, Lines 34-38 in Nishida et al. when considering 4,996,600 as prior art.*

As to claim **6**, Sauer et al., as modified by Kokie et al. and Pain et al., teaches an image sensor according to claim 3 (see 103(a) rejection above). The claim differs from Sauer et al., as modified by Kokie et al. and Pain et al., in that it requires interlace means adapted to produce video output from said image sensor in an interlace mode.

In the same field of endeavor, Nishida et al. teaches an interlace means (see Figure 15, Reference Numbers "103, "114") adapted to produce video output from said image sensor (see Col. 3, Lines 26-34) in an interlace mode (see Figure 1). In light of the teaching of Nishida et al. it would have been obvious to one of ordinary skill in the art at the time the invention was made to include interlace means adapted to produce video output from said image sensor in an interlace mode. Such a means would allow for a sufficiently large charge with little noise to be obtained, increased dynamic range and; consequently, high-quality reproduced images, with reduced residual images, can be obtained (see Nishida et al., Col. 2, Lines 43-48).

As to claim **7**, Sauer et al., as modified by Kokie et al., Pain et al., and Nishida et al., teaches that said interlace means comprise means adapted to activate said adjacent line means to combine charge of pairs of unit cells in adjacent lines beginning with odd lines (see Nishida et al., Figure 1, Reference Numbers "P1-1","P2-1" and "P3-1","P4-1"; sampling points in first field) adapted to an odd field output and of adjacent lines beginning with the even lines (see Nishida et al., Figure 1, Reference Numbers "P2-2","P3-2" and "P4-2","P5-2"; sampling points in second field) adapted to an even field output.

As to claim **17**, the limitations in claim 17 can be found in claim 6. Therefore, claim 17 has been analyzed and rejected as previously discussed with respect to claim 6.

As to claim **18**, the limitations in claim 18 can be found in claim 7. Therefore, claim 18 has been analyzed and rejected as previously discussed with respect to claim 7.

8. Claims 8-11,19-22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Sauer et al. and Kokie et al. (see Patent Numbers above), and further in view of Nishida et al (see Patent Number above). *Note the interchangeability of rows and columns in claims 8,9,19,20. Also note Col. 7, Lines 34-38 in Nishida et al. when considering 4,996,600 as prior art.*

As to claim **8**, Sauer et al., as modified by Kokie et al., teaches an image sensor of claim 4 (see 103(a) rejection above). The claim differs from Sauer et al., as modified by Kokie et al., in that it requires intercolumn means adapted to produce video output form said image sensor in an intercolumn mode.

In the same field of endeavor, Nishida et al. teaches an intercolumn means (see Figure 15, Reference Number "103","114") adapted to produce video output from said image sensor (see Col. 3, Lines 26-34) in an intercolumn mode (see Figure 6A and 6B). In light of the teaching of Nishida et al. it would have been obvious to one of ordinary skill in the art at the time the invention was made to include intercolumn means adapted to produce video output from said image sensor in an intercolumn mode. Such a means would allow for a sufficiently large charge with little noise to be obtained, increased dynamic range and; consequently, high-quality reproduced images, with reduced residual images, can be obtained (see Nishida et al., Col. 2, Lines 43-48).

As to claim **9**, Sauer et al., as modified by Kokie et al. and Nishida et al., teaches that said intercolumn means comprises means adapted to activate said adjacent column means to combine

charge of pairs of adjacent columns beginning with odd columns (see Figure 6B) adapted to an odd field output and of adjacent columns beginning with even columns (see Figure 6A) adapted an even field output.

As to claim **10**, Sauer et al., as modified by Kokie et al., teaches an image sensor according to claim 3 (see 103(a) rejection above). The claim differs from Sauer et al., as modified by Kokie et al., in that it requires block interlace means adapted to produce video output from said image sensor in an block interlace mode.

In the same field of endeavor, Nishida et al. teaches an block interlace means (see Figure 15, Reference Number "103","114") adapted to produce video output from said image sensor (Col. 3, Lines 26-34) in an block interlace mode (see Figure 1). In light of the teaching of Nishida et al. it would have been obvious to one of ordinary skill in the art at the time the invention was made to include block interlace means adapted to produce video output from said image sensor in an block interlace mode. Such a means would allow for a sufficiently large charge with little noise to be obtained, increased dynamic range and; consequently, high-quality reproduced images, with reduced residual images, can be obtained (see Nishida et al., Col. 2, Lines 43-48).

As to claim **11**, Sauer et al., as modified by Kokie et al and Nishida et al., teaches that said block interlace means comprise means adapted to activate said block means to combine charge of 2x2 blocks wherein the blocks of an odd field output begin with the block whose upper-left hand unit cell is in the first column, first line (see Figure 1, sampling points in the first field) and wherein the blocks of an even field output begin with the block whose upper-left hand unit cell is in the second column, second line (see Figure 1, sampling points of second field).

As to claim **19**, the limitations in claim 19 can be found in claim 8. Therefore, claim 19 has been analyzed and rejected as previously discussed with respect to claim 8.

As to claim **20**, the limitations in claim 20 can be found in claim 9. Therefore, claim 20 has been analyzed and rejected as previously discussed with respect to claim 9.

As to claim **21**, the limitations in claim 21 can be found in claim 10. Therefore, claim 21 has been analyzed and rejected as previously discussed with respect to claim 10.

As to claim **22**, the limitations in claim 22 can be found in claim 11. Therefore, claim 22 has been analyzed and rejected as previously discussed with respect to claim 11.

9. Claims 25,36 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Sauer et al. (see Patent Number above) in view of Pain et al. (see patent Number above). *Note the interchangeability of rows and columns in claims 25,36.*

As to claim **25**, Sauer et al. teaches a method according to claim 23 (see 102(b) rejection above), wherein summing comprises activation of certain lines and columns thereby to combine charge from the corresponding lines or columns, but the claim differs from Sauer et al. in that it requires, specifically, the activation of least two lines and the selection of one column thereby to combine charge from the corresponding unit cells in adjacent lines.

In the same field of endeavor, Pain et al. teaches the activation at least two adjacent lines and the selection of one column thereby to combine charge from the corresponding unit cells in adjacent lines (see Col. 2, Lines 59-67, Col. 3, Lines 1-9). In light of the teaching of Pain et al. it would have been obvious to one of ordinary skill in the art at the time the invention was made to activate a column and at least two adjacent lines, whereupon charges are combined from the

corresponding unit cells in the at least two adjacent lines. Such activations would allow for two methods of combining charges to be used, 1) activation of two columns and one line and summing, 2) activation of one column and two lines and summing; thus, receiving different signal-to-noise ratios for each method, comparing them, and using the highest to have a device with a more optimal signal-to-noise ratio with little or no change in resolution.

As to claim **36**, the limitations in claim 36 can be found in claim 25. Therefore, claim 36 has been analyzed and rejected as previously discussed with respect to claim 25.

10. Claims 28,29,39,40 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Sauer et al. and Pain et al. (see Patent Numbers above), and further in view of Nishida et al. (see Patent Number above). *Note the interchangeability rows and columns in claims 28,29,39,40. Also note Col. 7, Lines 34-38 in Nishida et al. when considering 4,996,600 as prior art.*

As to claim **28**, Sauer et al., as modified by Pain et al., teaches a method according to claim 25 (see 103(a) rejection above), but the claim differs from Sauer et al., as modified by Pain et al., in that the method comprises producing video output from said image sensor in an interlace mode.

In the same field of endeavor, Nishida et al. teaches producing video output from said image sensor (see Col. 3, Lines 26-34) in an interlace mode (see Figure 1). In light of the teaching of Nishida et al., it would have been obvious to one of ordinary skill in the art at the time the invention was made to produce video output from said image sensor in an interlace mode. . Such a modification would allow for a sufficiently large charge with little noise to be

obtained, increased dynamic range and; consequently, high-quality reproduced images, with reduced residual images, can be obtained (see Nishida et al., Col. 2, Lines 43-48).

As to claim **29**, Sauer et al., as modified by Pain et al. and Nishida et al., teaches a method according to claim 28 (see 103(a) rejection above) and wherein said producing comprises combining charge of pairs of unit cells in adjacent lines beginning with odd lines (see Nishida et al., Figure 1, Reference Numbers "P1-1","P2-1" and "P3-1","P4-1"; sampling points in first field) for an odd field output and of adjacent lines beginning with even lines (see Nishida et al., Figure 1, Reference Numbers "P2-2","P3-2" and "P4-2","P5-2"; sampling points in second field) for an even field output.

As to claim **39**, the limitations in claim 39 can be found in claim 28. Therefore, claim 39 has been analyzed and rejected as previously discussed with respect to claim 28.

As to claim **40**, the limitations in claim 40 can be found in claim 29. Therefore, claim 40 has been analyzed and rejected as previously discussed with respect to claim 29.

11. Claims 30-33, 41-44 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Sauer et al. in view of Nishida et al. (see Patent Numbers above). *Note the interchangeability of rows and columns in claims 30-33, 41-44. Also note Col. 7, Lines 34-38 in Nishida et al. when considering 4,996,600 as prior art.*

As to claim **30**, Sauer et al. teaches a method according to claim 26 (see 102(b) rejection), but the claim differs from Sauer et al. in that the method comprises producing video output from said image sensor in an intercolumn mode.

In the same field of endeavor, Nishida et al. teaches producing video output from said image sensor (see Col. 3, Lines 26-34) in an intercolumn mode (see Figure 6A and 6B). In light of the teaching of Nishida et al., it would have been obvious to one of ordinary skill in the art at the time the invention was made to produce video output from said image sensor in an intercolumn mode. Such a modification would allow for a sufficiently large charge with little noise to be obtained, increased dynamic range and; consequently, high-quality reproduced images, with reduced residual images, can be obtained (see Nishida et al., Col. 2, Lines 43-48).

As to claim **31**, Sauer et al., as modified by Nishida et al., teaches a method according to claim 30 (see 103(a) rejection above) and wherein said producing comprises combining charge of pairs of adjacent columns beginning with odd columns (see Figure 6B) for an odd field output and of adjacent columns beginning with even columns (see Figure 6A) for an even field output.

As to claim **32**, Sauer et al., as modified by Nishida et al., teaches a method according to claim 31 (see 103(a) rejection above), but the claim differs from Sauer et al., as modified by Nishida et al., in that the method requires producing video output from said image sensor in a block interlace mode.

In the same field of endeavor, Nishida et al., also teaches producing video output from said image sensor (see Col. 3, Lines 26-34) in a block interlace mode (see Figure 1). In light of the teaching of Nishida et al., it would have been obvious to one of ordinary skill in the art at the time the invention was made to produce video output from said image sensor in an block interlace mode. Such a modification would allow for a sufficiently large charge with little noise to be obtained, increased dynamic range and; consequently, high-quality reproduced images, with reduced residual images, can be obtained (see Nishida et al., Col. 2, Lines 43-48).

As to claim **33**, Sauer et al., as modified by Nishida et al., teaches a method according to claim 32 (see 103(a) rejection above) and wherein said producing comprises combining charge of 2x2 blocks wherein the blocks of an odd field output begin with the block whose upper-left hand unit cell is in the first column, first line (see Figure 1, sampling points in the first field) and wherein the blocks of an even field output begin with the block whose upper-left hand unit cell is in the second column, second line (see Figure 1, sampling points of second field).

As to claim **41**, the limitations in claim 41 can be found in claim 30. Therefore, claim 19 has been analyzed and rejected as previously discussed with respect to claim 30.

As to claim **42**, the limitations in claim 42 can be found in claim 31. Therefore, claim 42 has been analyzed and rejected as previously discussed with respect to claim 31.

As to claim **43**, the limitations in claim 43 can be found in claim 32. Therefore, claim 43 has been analyzed and rejected as previously discussed with respect to claim 32.

As to claim **44**, the limitations in claim 44 can be found in claim 33. Therefore, claim 44 has been analyzed and rejected as previously discussed with respect to claim 33.

### *Conclusion*

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony J. Daniels whose telephone number is (571) 272-7362. The examiner can normally be reached on 8:00 A.M. - 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AD
6/28/2005

NGOC-YEN VU
PRIMARY EXAMINER